R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

OBJECTION TO THE DRAWINGS

The objection to the drawings is respectfully traversed and should be withdrawn. A PTO-948 form has not been provided with the Office Action to indicate what informalities should be corrected. Furthermore, the form paragraph 6.21 (see MPEP §608.02(b)) reproduced in the Office Action fails to identify what defect has been discovered in the content of the drawings. Therefore, the Examiner is respectfully requested to either (i) provide a PTO-948 form identifying the informalities, (ii) identify the detects discovered in the contents of the drawings or (iii) withdraw the objection.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-20 under 35 U.S.C. §102(b) as being anticipated by Vegesna et al. '142 (hereafter Vegesna) is respectfully traversed and should be withdrawn.

The Federal Circuit has stated that "[t]o anticipate, ***every element and limitation*** of the claimed invention must be found in a single prior art reference, ***arranged as in the claim.***"[1]

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[1] *Brown v. 3M*, 60 USPQ2d 1375, 1376 (Fed. Cir. 2001) citing *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383, 58 USPQ2d 1286, 1291 (Fed. Cir. 2001); *Scripps Clinic & Research*

(Emphasis added). The Federal circuit has added that the anticipation determination is viewed from one of ordinary skill in the art: "There must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention."[2] Furthermore, "A claim is anticipated only if each and every element as set forth in the claim is found, either ***expressly or inherently*** described, in a single prior art reference."[3] (Emphasis added).

Vegesna concerns high performance register file with overlapping windows (Title).

Claim 1 provides (in part) a control circuit configured to store a plurality of register states. Despite the assertion on page 3 of the Office Action, FIG. 6, FIG. 8, column 2 lines 14-25 and column 10 lines 43-64 of Vegesna do not appear to **expressly** disclose storing register states in a Result Vector Driver 68 (asserted similar to the claimed control circuit). Furthermore, the Office Action makes no argument that storing register states is somehow **inherent** to the Results Vector Driver 68 of Vegesna. Therefore, *prima facie* anticipation has not been established.

Found. v. Genentech Inc., 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991) (Emphasis added by Appellant).

[2] *Scripps Clinic & Research Found. v. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991).

[3] *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, USPQ2d 1051, 1053 (Fed Circ. 1987).

Assuming, *arguendo*, that the Office Action is arguing for inherency (for which Applicant's representative does not necessarily agree), certainty for storing in the Result Vector Driver 68 has not been established even through inherency requires certainty of results, not mere possibility.[4] In particular, the Result Vector Driver 68 appears to be a form of demultiplexer based on a description in column 10 line 64 thru column 11 line 3 of Vegesna:

> The Result Vector Driver 68 takes incoming results data over thirty-two bit bus RESULT 88 and, in accordance with the one active Select R 92 line out of thirty-two, transmits the data to the appropriate thirty-two bit vector which form the inputs to the one of thirty-two memory locations in the current window of RAM Array 70 which is to have the result stored within it.

Appendix A provides a conventional definition of a demultiplexer is as follows:

> A *demultiplexer* is a circuit that receives information on a single line and transmits this information on one of 2^n possible output lines. The selection of a specific output line is controlled by the bit values of n selection lines.[5]

The Result Vector Driver 68 of Vegesna may be implemented with 32 demultiplexers, one for each line of a signal RESULT. Since the conventional demultiplexer defined above does not store data, the Result Vector Driver 68 of Vegesna does not necessarily store data. As such, no inherency exists in the Result Vector Driver 68 for

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[4] See, e.g., *Ethyl Molded Products Co. v. Betts Package, Inc.*, 9 U.S.P.Q. 2d 1001 (E.D.Ky 1988). See also, In re Oelrich, 666 F.2d 578, 581, 212 USPQ 323, 326 (C.C.P.A. 1981).

[5] Digital Logic and Computer Design, M. Morris Mano, 1979, pages 172-173.

storing a plurality of register states as presently claimed. Therefore, *prima facie* anticipation has not been established.

Furthermore, the Result Vector Driver 68 of Vegesna does not appear to be aware of a state of the registers 70. In particular, Appendix B provides a conventional definition of "state" as follows:

> The condition at a particular time of any of numerous elements of computing - a device, a communications channel, a network station, a program, a bit, or other element - used to report on or to control computer operations.[6]

In contrast, column 10, lines 54-64 of Vegesna refers to the registers has four types, "global", "local" "odd-result" and "even-result". As used in Vegesna, "types" does not appear to match the conventional definition for "states". Furthermore, no convincing line of reasoning is provided in the Office Action why one of ordinary skill in the art would consider the register types from Vegesna to be similar to similar to the claimed register states. As such, the assertion on page 3 of the Office Action that the Result Vector Driver 68 of Vegesna "holds the different types of register, or register states" is merely a conclusory statement lacking any supporting evidence. Therefore, *prima facie* anticipation has not been established.

Claim 1 further provides that the control circuit is configured to store a segment count signal. Despite the assertion on page 3 of the Office Action, column 3 lines 51-56 and column 3

---

[6] *Microsoft Computer Dictionary*, Fifth Edition, 2002, definition of "state" and "status"

lines 32-36 of Vegesna appear to be silent regarding the Result Vector Driver 68 (asserted similar to the claimed control circuit) storing a signal CWP (asserted similar to the claimed segment count signal) as presently claimed. Furthermore, the Office Action appears to be arguing that Vegesna discloses a structure different from as claimed where the signal CWP is stored outside the Result Vector Driver 68. Therefore, *prima facie* anticipation has not been established.

Claim 1 further provides that (A) the control circuit is configured to present a segment address signal (B) responsive to (i) the plurality of register states, (ii) a segment count signal and (iii) a register address signal. Despite the assertion on page 3 of the Office Action, (A) the signals on lines 106-112 of Vegesna are not presented from the Result Vector Driver 68 (asserted similar to the claimed control circuit). Furthermore, (B) Vegesna appears to be silent and no convincing line of reasoning is provided in the Office Action that the signals on lines 106-112 of Vegesna (asserted similar to the claimed segment address signal) are responsive to (i) information stored in the Result Vector Driver 68 (asserted to be aware of data similar to the claimed register states) and (iii) the signal ADDR (asserted similar to the claimed register address signal) as presently claimed. Therefore, *prima facie* anticipation has not been established. Claim 15 provides language similar to claim 1. As such, claims 1 and 15 are fully patentable over the cited reference and the rejection should be withdrawn.

Claim 10 provides a step for comparing a register address with a plurality of register states to present a gating signal. Page 6 of the Office Action asserts that (i) the Result Vector Driver 68 of Vegesna performs the claimed comparing, (ii) the Result Vector Driver 68 is aware of "resister states" and (iii) the ADDR signal on line 90 of Vegesna is similar to the claimed register address. In contrast, per the arguments presented above for claim 1, the Office Action has not established that the Result Vector Driver 68 is aware of register states. Furthermore, FIG. 8 of Vegesna shows that the Result Vector Driver 68 does not even receive the signal ADDR (asserted similar to the claimed register address). Therefore, *prima facie* anticipation has not been established.

Claim 10 further provides a step for gating a segment count with a gating count signal to present a segment address. In contrast, the Office Action asserts on page 6 that (i) signals presented from the Result Vector Driver 68 and (ii) signals on lines 106 and 108 are both similar to the claimed segment count. Since the Office Action is making conflicting statements regarding the alleged source of the claimed segment count, *prima facie* anticipation has not been established.

Furthermore, Vegesna appears to be silent regarding a gating function. Appendix C provides a common definition of "gating" as follows:

> The process of selecting only those portions of a wave between specified time intervals or between specified amplitude limits.[7]

No evidence is presented and no convincing line of reasoning is provided in the Office Action for a conventional gating function in Vegesna. Therefore, *prima facie* anticipation has not been established.

Assuming, *arguendo*, that signals presented from the Result Vector Driver 68 of Vegesna are similar to the claimed segment count (for which Applicant's representative does not necessarily agree), Vegesna appears to be silent and no convincing line of reasoning is provided in the Office Action where Vegesna expressly or inherently discloses that some of the signals generated by the Result Vector Driver 68 are gated by another signal presented from the Result Vector Driver 68, similar to the present claim. Therefore, *prima facie* anticipation has not been established.

Assuming, *arguendo*, that signals presented on lines 106 and 108 of Vegesna are similar to the claimed segment count (for which Applicant's representative does not necessarily agree), Vegesna appears to be silent and no convincing line of reasoning is provided in the Office Action where Vegesna expressly or inherently discloses that the signals on lines 106 and 108 are gated by a signal presented from the Result Vector Driver 68, similar to the

[7] www.TutorGig.com, Encyclopedia definition 1.

present claim. Therefore, *prima facie* anticipation has not been established.

Claim 10 further provides a step for addressing a register stack with the register address and the segment address. Page 6 of the Office Action argues that the registers 70 of Vegesna are addressed by "part of the segment address signal" from the Result Vector Generator 68 and another "part of the segment address signal" on lines 106 and 108. In contrast, Vegesna appears to be silent and no argument is presented in the Office Action that the registers 70 of Vegesna are addressed **with** the signal ADDR (asserted similar to the claimed register address) as presently claimed. Therefore, *prima facie* anticipation has not been established. As such, the claim 10 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 16 provides that the control circuit comprises a counter configured to present the segment count signal. In contrast, Vegesna appears to be silent and the arguments on page 8 of the Office Action fail to establish that the Result Vector Driver 68 of Vegesna (asserted similar to the claimed control circuit) includes a counter configured to generate the signal CWP (asserted similar to the claimed segment count signal) as presently claimed. Therefore, *prima facie* obviousness has not been established.

Claim 17 provides that the control circuit further comprises (i) (from claim 5) a status circuit configured to present the gating signal in response to the register address signal and

(ii) (from claim 17) a plurality of logic gates configured to present the segment address signal responsive to the gating signal and the segment count signal. The arguments against claim 5 on page 4 of the Office Action assert that the gating signal is presented from a store register decode logic 76 of Vegesna. The arguments against claim 17 on page 8 of the Office Action conflict with the arguments against claim 5 by asserting that the gating signal is presented from the Result Vector Driver 68 of Vegesna. Since the Office Action is using conflicting arguments against claim 17 (when incorporating the limitations of claim 5), *prima facie* obviousness has not been established.

Furthermore, Vegesna appears to be silent and the arguments on page 8 of the Office Action fail to establish that the Result Vector Driver 68 of Vegesna comprises logic gates configured to present the segment address signal responsive to the gating signal and the segment count signal as presently claimed. Therefore, *prima facie* obviousness has not been established.

Claim 18 provides a step of presenting the segment address as a predetermined address responsive to the gating signal having a global state. In contrast, Vegesna appears to be silent and the Office Action makes no argument that a signal presented from the Result Vector Driver 68 or store register decode logic 76 of Vegesna (asserted similar to the claimed gating signal) has a global state. Therefore, *prima facie* obviousness has not been established.

Claim 19 provides a step of storing the register state prior to comparing (with a register address). As asserted above for claim 1, the Office Action has failed to establish that the Vegesna expressly or inherently discloses storing register states as presently claimed. Therefore, *prima facie* obviousness has not been established.

IMPROPERLY EXPRESSED REJECTIONS

Applicant's representative respectfully requests that a next set of rejections, if any, be presented in a non-final Office Action due to a lack of proper development for the rejections. MPEP §707.07(f) reads:

> Where the applicant traverses any rejection, the examiner should, if he or she repeats the rejection, take note of the applicant's argument and **answer the substance** of it. (Emphasis added)

The current Office Action repeats the rejections for claims 6, 7, 8, 11 and 12 yet does not answer the substance of the traverses made in the June 18, 2004 Amendment. As such, the current Office Action is incomplete.

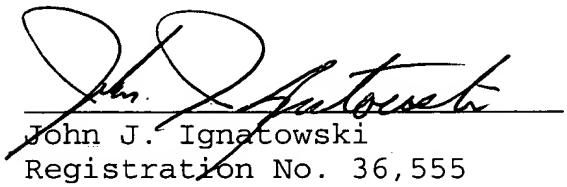
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicant's representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



John J. Ignatowski
Registration No. 36,555

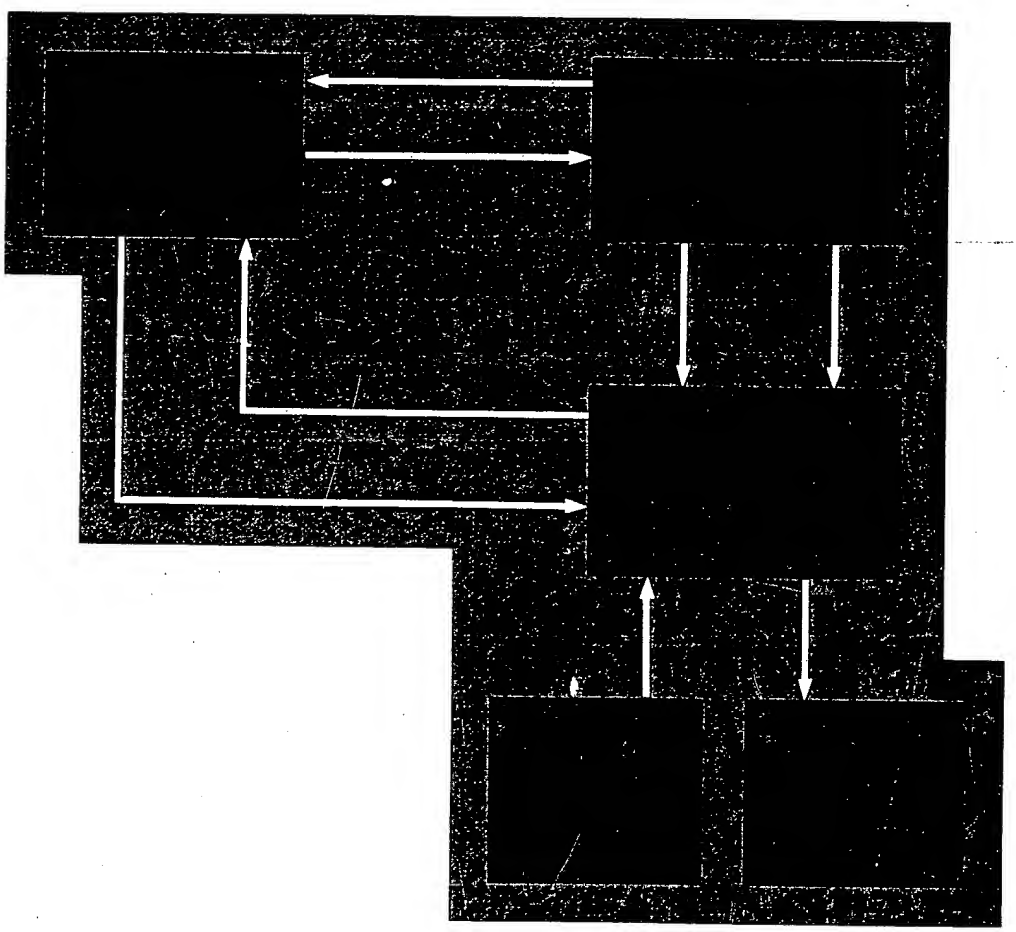
Dated: November 19, 2004

c/o Pete Scott
LSI Logic Corporation
1621 Barber Lane, M/S D-106 Legal
Milpitas, CA 95035

Docket No.: 99-339 / 1496.00059

Appendix A

Digital Logic and Computer Design



M. MORRIS MANO

Library of Congress Cataloging in Publication Data

MANO, M. MORRIS (date)
Digital logic and computer design.

Bibliography: p.
Includes index.
1.–Electronic digital computers. 2.–Logic circuits. 3.–Digital integrated circuits. 4.–Logic design. I.–Title.
TK7888.3.M345 621.3815'3 78-21462
ISBN 0-13-214510-3

Printed in the United States of America

10 9 8 7 6 5 4 3 2 1

Editorial/Production Supervision by Lynn S. Frankel
Cover Design by Edsal Enterprise
Manufacturing Buyer: Gordon Osbourne

PRENTICE-HALL INTERNATIONAL, INC., *London*
PRENTICE-HALL OF AUSTRALIA PTY. LIMITED, *Sydney*
PRENTICE-HALL OF CANADA, LTD., *Toronto*
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complemented form F' with $2^n - k$ minterms. If the number of minterms in a function is greater than $2^n/2$, then F' can be expressed with fewer minterms than required for F. In such a case, it is advantageous to use a NOR gate to sum the minterms of F'. The output of the NOR gate will generate the normal output F.

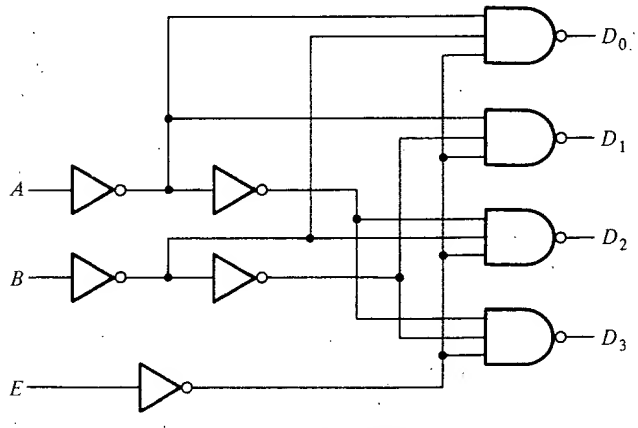
The decoder method can be used to implement any combinational circuit. However, its implementation must be compared with all other possible implementations to determine the best solution. In some cases this method may provide the best implementation, especially if the combinational circuit has many outputs and if each output function (or its complement) is expressed with a small number of minterms.

Demultiplexers

Some IC decoders are constructed with NAND gates. Since a NAND gate produces the AND operation with an inverted output, it becomes more economical to generate the decoder minterms in their complemented form. Most, if not all, IC decoders include one or more *enable* inputs to control the circuit operation. A 2-to-4 line decoder with an enable input constructed with NAND gates is shown in Fig. 5-12. All outputs are equal to 1 if enable input E is 1, regardless of the values of inputs A and B. When the enable input is 0, the circuit operates as a decoder with complemented outputs. The truth table lists these conditions. The X's under A and B are don't-care conditions. Normal decoder operation occurs only with $E = 0$, and the outputs are selected when they are in the 0 state.

The block diagram of the decoder is shown in Fig. 5-13(a). The small circle at input E indicates that the decoder is enabled when $E = 0$. The small circles at the outputs indicate that all outputs are complemented.

A decoder with an enable input can function as a demultiplexer. A *demultiplexer* is a circuit that receives information on a single line and transmits this information on one of 2^n possible output lines. The selection of a specific output

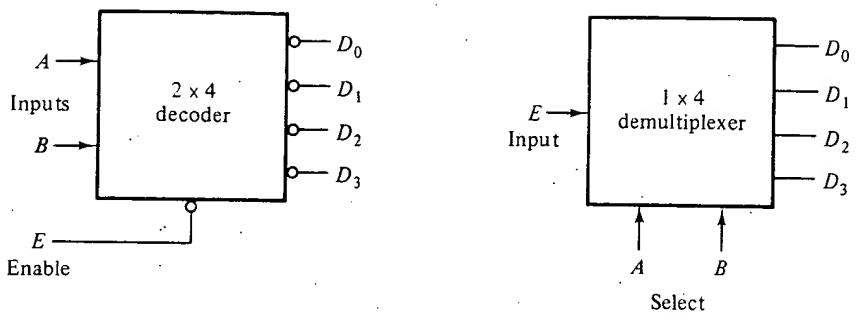


(a) Logic diagram.

E	A	B	D_0	D_1	D_2	D_3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

(b) Truth table

Figure 5-12 A 2-to-4 line decoder with enable (E) input



(a) Decoder with enable

(b) Demultiplexer

Figure 5-13 Block diagrams for the circuit of Fig. 5-12

line is controlled by the bit values of n selection lines. The decoder of Fig. 5-12 can function as a demultiplexer if the E line is taken as a data input line and lines A and B are taken as the selection lines. This is shown in Fig. 5-13(b). The single input variable E has a path to all four outputs, but the input information is directed to only one of the output lines, as specified by the binary value of the two selection lines A and B. This can be verified from the truth table of this circuit, shown in Fig. 5-12(b). For example, if the selection lines $AB = 10$, output D_2 will be the same as the input value E, while all other outputs are maintained at 1. Because decoder and demultiplexer operations are obtained from the same circuit, a decoder with an enable input is referred to as a *decoder/demultiplexer*. It is the enable input that makes the circuit a demultiplexer; the decoder itself can use AND, NAND, or NOR gates.

Decoder/demultiplexer circuits can be connected together to form a larger decoder circuit. Figure 5-14 shows two 3×8 decoders with enable inputs connected to form a 4×16 decoder. When $w = 0$, the top decoder is enabled and the

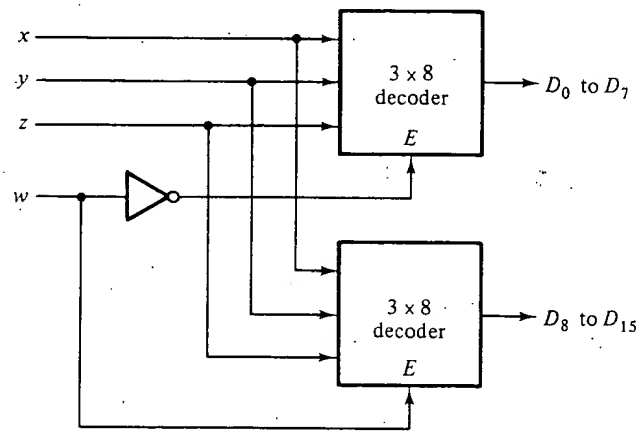


Figure 5-14 A 4×16 decoder constructed with two 3×8 decoders

A-4

Appendix B

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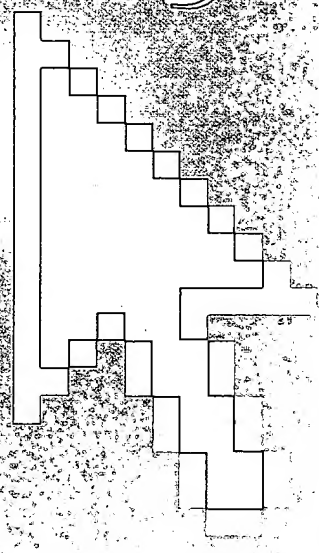

PUBLISHED BY
Microsoft Press
A Division of Microsoft Corporation
One Microsoft Way
Redmond, Washington 98052-6399

Library of Congress Cataloging-in-Publication Data
Microsoft Computer Dictionary.--5th ed.
p. cm.
ISBN 0-7356-1495-4
1. Computers--Dictionaries. 2. Microcomputers--Dictionaries.

AQ76.5. M52267 2002
004'.03--dc21 200219714

Printed and bound in the United States of America.

2 3 4 5 6 7 8 9 QWT 7 6 5 4 3 2

Distributed in Canada by H.B. Fenn and Company Ltd.

A CIP catalogue record for this book is available from the British Library.

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B-2

start/stop transmission *n. See* asynchronous transmission.

startup *n. See* boot[1].

startup application *n.* On the Macintosh, the application that takes control of the system when the computer is turned on.

STARTUP.CMD *n.* A special-purpose batch file stored in the root directory of the startup disk in OS/2—the OS/2 equivalent of an MS-DOS AUTOEXEC.BAT file.

startup disk *n. See* system disk.

startup ROM *n.* The bootstrap instructions coded into a computer's ROM (read-only memory) and executed at startup. The startup ROM routines enable a computer to check itself and its devices (such as the keyboard and disk drives), prepare itself for operation, and run a short program to load an operating-system loader program. *See also* boot[1], power-on self test.

startup screen *n.* A text or graphics display that appears on the screen when a program is started (run). Startup screens usually contain information about the software's version and often contain a product or corporate logo.

star-wired ring *n.* A network topology in which hubs and nodes connect to a central hub in typical star fashion, but the connections within the central hub form a ring. Star-wired ring is a combination of star and ring topologies.

state *n. See* status.

stateful *adj.* Of or pertaining to a system or process that monitors all details of the state of an activity in which it participates. For example, stateful handling of messages takes account of their content. *Compare* stateless.

stateless *adj.* Of or pertaining to a system or process that participates in an activity without monitoring all details of its state. For example, stateless handling of messages might take account of only their sources and destinations but not their content. *Compare* stateful.

statement *n.* The smallest executable entity within a programming language.

state-of-the-art *adj.* Up to date; at the forefront of current hardware or software technology.

static[1] *adj.* In information processing, fixed or predetermined. For example, a static memory buffer remains invariant in size throughout program execution. The opposite condition is *dynamic*, or ever-changing.

static[2] *n.* In communications, a crackling noise caused by electrical interference with a transmitted signal. *See also* noise (definition 2).

static allocation *n.* Apportionment of memory that occurs once, usually when the program starts. The memory remains allocated during the program's execution and is not deallocated until the program is finished. *See also* allocate, deallocate. *Compare* dynamic allocation.

static binding *n.* Binding (converting symbolic addresses in the program to storage-related addresses) that occurs during program compilation or linkage. *Also called:* early binding. *Compare* dynamic binding.

static buffer *n.* A secondary sound buffer that contains an entire sound; these buffers are convenient because the entire sound can be written once to the buffer. *See also* streaming buffer.

static electricity *n.* An electrical charge accumulated in an object. Although generally harmless to humans, the discharge of static electricity through an electronic circuit can cause severe damage to the circuit.

static RAM *n.* A form of semiconductor memory (RAM) based on the logic circuit known as a flip-flop, which retains information as long as there is enough power to run the device. Static RAMs are usually reserved for use in caches. *Acronym:* SRAM. *See also* cache, RAM, synchronous burst static RAM. *Compare* dynamic RAM.

static routing *n.* Routing based on a fixed forwarding path. Unlike dynamic routing, static routing does not adjust to changing network conditions. *Compare* dynamic routing.

static Web page *n.* Web page that displays the same content to all viewers. Usually written in hypertext markup language (HTML), a static Web page displays content that changes only if the HTML code is altered. *See also* dynamic Web page.

station *n.* **1.** In the IEEE 802.11 wireless LAN specification, a single, often mobile, node. **2.** *See* workstation.

stationery[1] *adj.* Describing a type of document that, when opened by the user, is duplicated by the system; the copy is opened for the user's modification while the original document remains intact. Stationery documents can be used as document templates or boilerplates. *See also* boilerplate, template (definition 5).

stationery[2] *n.* A stationery document. *See also* stationery[1].

B-3

statistical multiplexer *n.* A multiplexing device that adds intelligence to time-division multiplexing by using buffering (temporary storage) and a microprocessor to combine transmission streams into a single signal and to allocate available bandwidth dynamically. *Also called:* stat mux. *See also* dynamic allocation, multiplexing, time-division multiplexing.

statistics *n.* The branch of mathematics that deals with the relationships among groups of measurements and with the relevance of similarities and differences in those relationships. *See also* binomial distribution, Monte Carlo method, probability, regression analysis, standard deviation, stochastic.

stat mux *n. See* statistical multiplexer.

status *n.* The condition at a particular time of any of numerous elements of computing—a device, a communications channel, a network station, a program, a bit, or other element—used to report on or to control computer operations.

status bar *n.* In Windows 9x and Windows NT 4 and later, a space at the bottom of many program windows that contains a short text message about the current condition of the program. Some programs also display an explanation of the currently selected menu command in the status bar. See the illustration.

Status bar.

status codes *n.* Strings of digits or other characters that indicate the success or failure of some attempted action. Status codes were commonly used to report the results of early computer programs, but most software today uses words or graphics. Internet users, especially those with UNIX shell accounts, are likely to encounter status codes while using the Web or FTP. *See also* HTTP status codes.

steganography *n.* A "hide-in-plain-sight" technique for concealing information by embedding a message within an innocuous cover message. In steganography, bits of unnecessary data within an image, sound, text, or even a blank file are replaced with bits of invisible information. The term steganography comes from the Greek for "covered writing" and has traditionally included any method of secret communication that conceals the existence of the message. Because steganography cannot be detected by decryption software, it is often used to replace or supplement encryption.

step-frame *n.* The process of capturing video images one frame at a time. This process is used by computers that are too slow to capture analog video images in real time.

stepper motor *n.* A mechanical device that rotates only a fixed distance each time it receives an electrical pulse. A stepper motor is part of a disk drive.

step-rate time *n.* The time required to move a disk actuator arm from one track to the next. *See also* actuator, stepper motor.

stereogram *n. See* autostereogram.

sticky *adj.* In reference to a Web site, properties such as targeted content or services that increase the amount of time users choose to spend at the site and increase user's desire to return to the site repeatedly.

StickyKeys *n.* An accessibility feature built into Macintosh and Windows computers that causes modifier keys such as Shift, Control, or Alt to "stay on" after they are pressed, eliminating the need to press multiple keys simultaneously. This feature facilitates the use of modifier keys by users who are unable to hold down one key while pressing another.

stochastic *adj.* Based on random occurrences. For example, a stochastic model describes a system by taking into account chance events as well as planned events.

stop bit *n.* In asynchronous transmission, a bit that signals the end of a character. In early electromechanical teleprinters, the stop bit provided time for the receiving mechanism to coast back to the idle position and, depending on the mechanism, had a duration of 1, 1.5, or 2 data bits. *See also* asynchronous transmission. *Compare* parity bit, start bit.

Stop error *n.* A serious error that affects the operating system and that could place data at risk. The operating system generates an obvious message, a screen with the Stop error, rather than continuing on and possibly corrupting data. *Also called:* blue screen error, fatal system error. *See also* Blue Screen of Death.

storage *n.* In computing, any device in or on which information can be kept. Microcomputers have two main types of storage: random access memory (RAM) and disk drives and other external storage media. Other types of storage include read-only memory (ROM) and buffers.

storage area network *n.* A high-speed network that provides a direct connection between servers and storage, including shared storage, clusters, and disaster-recovery

B-4

Appendix C

Articles 1 - 14 of 14

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1. **Gating**
   In telecommunication , the term **gating** has the following meanings b 1. b The process of selecting only those portions of a wave between specified time intervals or between specified amplitude limits. b

2. National Speleological Society
   The National Speleological Society NSS is an organization formed to advance the exploration, conservation, study, and understanding of caves . Members may engage in mapping, cleaning, gating sensitive ...

3. Intensified charge-coupled device
   of **gating** the MCP also offers the possibility to gate ICCD cameras very fast. Therefore ICCD cameras

4. Frog (disambiguation)
   term referring to a French person. FROG stands for Frequency Resolved Optical **Gating**, a method

5. Significant condition
   , or **gating** . Source from Federal Standard 1037C and from MIL STD 188

6. Flow cytometry
   extractions which are termed gates. Specific **gating** protocols exist for diagnostic and clinical purposes

7. Time-resolved spectroscopy
   gating femtoseconds nanoseconds a short laser pulse acts as a gate for the detection of fluorescence

8. Connex
   with indequate electric power supplies, for **gating** and fencing stations to reduce freeloader

9. Proctor
   as **gating** . They have to draw up the list of candidates for examination, and have to be present at all ... number of days **gating** . In the case of more serious offences the proctor generally reports the matter

10. G protein
    molecule itself, by activating other second messengers or by **gating** ion channel s directly. For example

11. Nuclear medicine
    often called a dynamic dataset, a cardiac gated cardiac **gating** time sequence, or a spatial sequence

12. Classic RISC pipeline
    , generally by **gating** off the clock to the flip flops at the start of each stage. The disadvantage of this strategy

13. Personal rapid transit
    the vehicle, the more costly the track, and the track is the **gating** system cost. As well, large tracks

14. List of electronics topics